**LESSON PLAN**

**Subject Code & Name: CPLD & FPGA**

**Branch: VLSI Class / Semester: IM.Tech -SEM II Academic Year: 2017-18**

**Faculty: B.Rama Rao**

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| **Period** | **Date (Tentative)** | **Topic** | **Unit No.** | **Teaching Methodology** | **Remarks** | **Corrective action upon review** |
|  |  | **PROGRAMMABLE LOGIC DEVICES** | **I** |  |  |  |
| 1 | 26.02.2018 | Introduction |  | Chalk & Talk |  |  |
| 2 | 27.02.2018 | ROM, PLA, PAL– Features |  | Chalk & Talk |  |  |
| 3 | 01.03.2018 | CPLD, FPGA – Features |  | Chalk & Talk |  |  |
| 4 | 02.03.2018 | Architectures of ROM, PLA, PAL |  | Chalk & Talk |  |  |
| 5 | 05.03.2018 | Programming |  | Chalk & Talk |  |  |
| 6 | 06.03.2018 | Applications of ROM, PLA, PAL |  | Chalk & Talk |  |  |
| 7 | 08.03.2018 | Implementation of MSI circuits using Programmable logic Devices. |  | Chalk & Talk |  |  |
|  |  | **CPLDs** | **II** |  |  |  |
| 8 | 09.03.2018 | Complex Programmable Logic Devices, Altera series |  | Chalk & Talk |  |  |
| 9 | 12.03.2018 | Max 5000/7000 series and Altera FLEX logic |  | Chalk & Talk |  |  |
| 10 | 13.03.2018 | 10000 series CPLD AMD’s |  | Chalk & Talk |  |  |
| 11 | 15.03.2018 | CPLD (Mach 1 ,2), |  | Chalk & Talk |  |  |
| 12 | 16.03.2018 | CPLD (Mach 3,4), |  |  |  |  |
| 13 | 19.03.2018 | CPLD (Mach 5), |  |  |  |  |
| 14 | 20.03.2018 | Cypress FLASH 370 Device technology, |  | Chalk & Talk |  |  |
| 15 | 22.03.2018 | Lattice pLSI’s architectures –3000 series |  | Chalk & Talk |  |  |
| 16 | 23.03.2018 | Speed performance and in system programmability |  | Chalk & Talk |  |  |
|  |  | **FPGAs** | **III** |  |  |  |
| 17 | 26.03.2018 | Field Programmable Gate Arrays- |  | Chalk & Talk |  |  |
| 18 | 27.03.2018 | Logic blocks, |  | Chalk & Talk |  |  |
| 19 | 29.03.2018 | routing architecture, |  | Chalk & Talk |  |  |
| 20 | 30.03.2018 | design flow |  | Chalk & Talk |  |  |
| 21 | 02.04.2018 | technology mapping for FPGAs, |  | Chalk & Talk |  |  |
| 22 | 02.04.2018 | Xilinx XC22000 |  | Chalk & Talk |  |  |
| 23 | 03.04.2018 | Xilinx XC3000 |  |  |  |  |
| 24 | 05.04.2018 | Xilinx XC4000 |  |  |  |  |
| 25 | 06.04.2018 | ALTERA’s FPGA |  |  |  |  |
| 26 | 09.04.2018 | FLEX 8000/10000, FPGAs |  | Chalk & Talk |  |  |
| 27 | 10.04.2018 | FPGAs: AT &T ORCA’s |  |  |  |  |
|  |  | **FINITE STATE MACHINES (FSM)** | **IV** |  |  |  |
| 28 | 12.04.2018 | Top Down Design, State Transition Table, |  | Chalk & Talk |  |  |
| 29 | 13.04.2018 | State assignments for FPGAs, |  | Chalk & Talk |  |  |
| 30 | 16.04.2018 | Realization of state machine charts using PAL |  | Chalk & Talk |  |  |
| 31 | 17.04.2018 | Alternative realization for state machine charts using microprogramming, |  | Chalk & Talk |  |  |
| 32 | 24.04.2018 | linked state machine, encoded state machine. |  | Chalk & Talk |  |  |
| 33 | 26.04.2018 | FSM ARCHITECTURES: Architectures Centered around non registered PLDs, |  | Chalk & Talk |  |  |
| 34 | 27.04.2018 | Design of state machines centered around shift registers |  | Chalk & Talk |  |  |
| 35 | 04.06.2018 | One Hot state machine, |  | Chalk & Talk |  |  |
| 36 | 05.06.2018 | Petrinets for state machines-Basic concepts and properties, |  | Chalk & Talk |  |  |
| 37 | 07.06.2018 | Finite State Machine-Case study. |  | Chalk & Talk |  |  |
|  |  | **DESIGN METHODS** | **V** |  |  |  |
| 38 | 08.06.2018 | Introduction |  | Chalk & Talk |  |  |
| 39 | 11.06.2018 | One –hot design method, |  | Chalk & Talk |  |  |
| 40 | 12.06.2018 | Use of ASMs in one-hot design method, |  | Chalk & Talk |  |  |
| 41 | 14.06.2018 | Applications of one hot design method, |  | Chalk & Talk |  |  |
| 42 | 15.06.2018 | Extended Petri-nets for parallelcontrollers, |  | Chalk & Talk |  |  |
| 43 | 18.06.2018 | Meta Stability, |  | Chalk & Talk |  |  |
| 44 | 19.06.2018 | Synchronization, |  | Chalk & Talk |  |  |
| 45 | 21.06.2018 | Complex design using shift registers. |  | Chalk & Talk |  |  |
|  |  | **SYSTEM LEVEL DESIGN** | **VI** |  |  |  |
| 46 | 22.06.2018 | Controller, data path designing, |  | Chalk & Talk |  |  |
| 47 | 25.06.2018 | Functional partition, |  | Chalk & Talk |  |  |
| 48 | 26.06.2018 | Digital front end digital design tools for FPGAs & ASICs, |  | Chalk & Talk |  |  |
| 49 | 28.06.2018 | System level design using mentor graphics EDA tool(FPGA Advantage), |  | Chalk & Talk |  |  |
| 50 | 29.06.2018 | Design flow using CPLDs and FPGAs. |  | Chalk & Talk |  |  |
| 51 | 02.07.2018 | CASE STUDIES: Design considerations using CPLDs of parallel adder |  | Chalk & Talk |  |  |
| 52 | 03.07.2018 | parallel adder sequential circuits, |  | Chalk & Talk |  |  |
| 53 | 05.07.2018 | counters |  | Chalk & Talk |  |  |
| 53 | 06.07.2018 | Multiplexers parallel Controllers |  | Chalk & Talk |  |  |
| 54 | 10.07.2018 | CASE STUDIES: Design considerations using FPGAs of parallel adder |  |  |  |  |
| 55 | 12.07.2018 | parallel adder sequential circuits, |  |  |  |  |
| 56 | 16.07.2018 | counters |  |  |  |  |
| 57 | 17.07.2018 | Multiplexers parallel Controllers |  |  |  |  |
| 58 | 20.07.2018 | CASE STUDIES: Design considerations using CPLDs and FPGAs of parallel adder |  |  |  |  |

**CR: CLASS ROOM PPT: POWER POINT PRESENTATION LCD**

**TEXT BOOKS:**

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.

2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.

3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

**REFERENCES BOOKS:**

1. Digital Design Using Field Programmable Gate Array, P.K.Chan& S. Mourad,1994, Prentice Hall.

2. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007,BSP.

**FACULTY HEAD OF THE DEPARTMENT**